ADFP Cloud 2.0

Cell-based 設計使用者手冊

2024.11.18 Version 1

Editor

賴林鴻

目錄

1. Run RLT/Gate/Post Simulation

1.1 模擬準備

(1) 需使用到的 verilog 檔案

將所有需要用到的檔案寫入 filelist.f

(2) 決定模擬的精細度

TIMESCALE=-timescale=1ns/1fs

1.2 RTL 模擬

(1) 相關路徑

如有使用 Design Ware IP 需 include

DW_SIM=/usr/cad/synopsys/synthesis/cur/dw/sim_ver/

為了讓 Verdi 軟體能正常打開波形

VERDI=/usr/cad/synopsys/verdi/2019.06/

(2) 使用 Synopsys VCS 進行 RTL 模擬

```
vcs ${TIMESCALE} -j${num_CPU_cores} -sverilog +v2k -full64 -
Mupdate -R -debug_access+all -y ${DW_SIM} +libext+.v
incdir+${DW_SIM} -f ${source_file} -o ${output_file} -l ${log_file}
-P ${VERDI}/share/PLI/VCS/linux64/novas.tab
${VERDI}/share/PLI/VCS/linux64/pli.a +define+RTL +notimingchecks
```

(3) 使用 Cadence xrun 進行 RTL 模擬

```
xrun -mcl ${num_CPU_cores} -f ${source_file} -y ${DW_SIM} -sv -
libext .v -loadpli1 debpli:novas_pli_boot -debug -notimingchecks -
define RTL
```

1.3 Gate-Level 模擬

(1) 相關路徑

Standard Cell-library Behavior Model

N16ADFP_SIM=/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/VERILOG/N16ADFP_StdCell.v

(2) 使用 VCS 進行 Gate 模擬

vcs ${TIMESCALE} -j${num_CPU_cores} -sverilog +v2k -full64 -Mupdate -R -debug_access+all -f ${source_file} -o ${output_file} -l ${log_file} -P ${VERDI}/share/PLI/VCS/linux64/novas.tab ${VERDI}/share/PLI/VCS/linux64/pli.a -v ${N16ADFP_SIM} +define+GATE +neg_tchk +nowarnNTCDSN

(3) 使用 Xrun 進行 Gate 模擬

xrun -mcl ${num_CPU_cores} -f ${source_file} -sdf_precision 1fs -v ${N16ADFP_SIM} -loadpli1 debpli:novas_pli_boot -debug -define GATE

1.4 Post-Level 模擬

(1) 相關路徑

Standard IO library Behavior Model

N16ADFP_IO_SIM=/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/VERILOG/N16ADFP_StdIO.v

(2) 使用 VCS 進行 Post 模擬

```
vcs ${TIMESCALE} -j${num_CPU_cores} -sverilog +v2k -full64 -Mupdate -R -debug_access+all -f ${source_file} -o ${output_file} -l ${log_file} -P ${VERDI}/share/PLI/VCS/linux64/novas.tab ${VERDI}/share/PLI/VCS/linux64/pli.a -v ${N16ADFP_SIM} -v ${N16ADFP_IO_SIM}+define+POST +neg_tchk
```

(3) 使用 Xrun 進行 Post 模擬

```
xrun -mcl ${num_CPU_cores} -f ${source_file} -sdf_precision 1fs -v ${N16ADFP_SIM} -v ${N16ADFP_IO_SIM} -loadpli1 debpli:novas_pli_boot -debug -define POST
```

1.5 使用 nWave 打開波形

```
nWave -ssf *.fsdb
```

1.6 使用 verdi 打開波形

```
verdi -ssf *.fsdb -sv -f ${source_file} -nologo+v2k –autoalias +define+RTL/GATE/POST
```

2. Run Logic Synthesis with Design Compiler

2.1 製程設定 .synopsys_dc.setup

(1) 相關路徑

Standard Cell library Behavior Model (CCS Model)

/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/CCS/

Standard Cell library Behavior Model (NLDM Model)

/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/NLDM/

Standard IO library Behavior Model (NLDM Model)

/ADFP/Executable_Package/Collaterals/IP/stdio/N16ADFP_StdIO/NLDM/N16ADFP_StdIO

target_library

N16ADFP_StdCellss0p72vm40c_ccs.db (slow case)

link_library

N16ADFP_SRAM_ss0p72v0p72vm40c_100a.db (memory)

(2) Command Line 指令

```
dcnxt_shell -f ${syn_tcl} -x "set_host_options -max_cores ${num_CPU_cores}" -output_log_file ${syn_log}
```

(3) GUI 指令

```
dcnxt_shell -f ${syn_tcl} -x "set_host_options -max_cores ${num_CPU_cores}" -output_log_file ${syn_log} -gui
```

3. Power Analysis with PrimeTime

3.1 Command Line 指令

```
pt_shell -f ${pt_tcl} -x "set_host_options -max_cores ${num_CPU_cores}"
-output_log_file ${pt_log}
```

4. 查看 TSMC 提供之 CB 文件範例練習

TSMC 有提供 Lab 供大家參考，特別是有關 Physical Design 有需多 Library 和 mmmc 檔案要設定，建議可以參考 Lab。路徑如下:

/ADFP/Executable_Package/Lab

請參閱家目錄的浮水印文件，有關 CB 說明:
~/Desktop/ADFP_PDF/

(1) ADFP046_TSMC_N16ADFP_Introduction_20220118_wmc.pdf

有關 TSMC ADFP 製程的簡要說明。

(2) **ADFP045_TSMC_N16ADFP_Chip_20220118_wmc.pdf**

有關 APR 需要注意的事項

(3) ADFP043_TSMC_N16ADFP_Lab_Chip_20220211_wmc.pdf

該文件提供 Lab 練習，使用 Innovus 跑 IP level 和 Full Chip level APR

5. 查看 NYCU 課程提供之 CB 文件範例練習

請參閱家目錄的浮水印文件，有關 CB 說明:
~/Desktop/ADFP_PDF/

(1) COURSE01_ICLAB_ADFP_FinFET_cell-based_tutorial_2024-01-10.pdf

有關 TSMC ADFP 製程的簡要說明。

(2) COURSE02_ICLAB_ADFP_FIFO_synthesis_tutorial_2024-01-10.pdf

有關如何 Step by step 跑完 Logic Synthesis 流程。

(3) COURSE03_ICLAB_ADFP_FIFO_APR_tutorial_2024-01-10.pdf

有關如何 Step by step 跑完 APR 流程。(尚未加入 sign-off)

Revision Record and Author List

Original Tutorial by 賴林鴻

2024.11.18 Version 1 edited by Lin-Hung Lai